

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD.,)	
)	
Plaintiff,)	
)	
v.)	Case No. 6:19-cv-00515-ADA
)	
GOOGLE LLC,)	
)	
Defendant.)	
)	
<hr/>		
SOLAS OLED LTD.,)	
)	
Plaintiff,)	
)	
v.)	Case No. 6:19-cv-00537-ADA
)	
APPLE INC.,)	
)	
Defendant.)	
)	
<hr/>		
SOLAS OLED LTD.,)	
)	
Plaintiff,)	
)	
v.)	Case No. 6:19-cv-00631-ADA
)	
HP INC.,)	
)	
Defendant.)	
)	

DEFENDANTS' AND INTERVENOR'S REPLY CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

	Page
I. U.S. PATENT NO. 7,446,338 (“338 PATENT”)	1
A. “TRANSISTOR ARRAY SUBSTRATE” (CLAIM 1).....	1
B. “PROJECT FROM A SURFACE OF THE TRANSISTOR ARRAY SUBSTRATE” (CLAIM 1)	3
II. U.S. PATENT NO. 7,499,042 (“042 PATENT”)	3
A. “SELECTION PERIOD” (CLAIM 1)	3
B. “SEQUENTIALLY SELECTS SAID PLURALITY OF SELECTION SCAN LINES IN EACH SELECTION PERIOD” (CLAIM 1).....	6
C. “DESIGNATING CURRENT” (CLAIM 1).....	7
D. “CURRENT LINES” (CLAIM 1)	8
III. U.S. PATENT NO. 7,663,615 (“615 PATENT”)	9
A. “THE OPERATION” (CLAIM 11)	9
B. “PRECHARGE VOLTAGE” (CLAIM 11).....	11
C. “WRITING CONTROL SECTION” (CLAIM 11)	12
D. “DATA LINES” (CLAIM 11)	13
IV. U.S. PATENT NO. 7,573,068 (“068 PATENT”)	15
A. “FORMED ON SAID PLURALITY OF SUPPLY LINES ALONG SAID PLURALITY OF SUPPLY LINES” (CLAIM 1) / “CONNECTED TO SAID PLURALITY OF SUPPLY LINES ALONG SAID PLURALITY OF SUPPLY LINES” (CLAIM 13).....	15
B. “SIGNAL LINES” / “SUPPLY LINES” (CLAIMS 1, 13)	17
C. “SOURCE” / “DRAIN” (CLAIMS 1, 13)	19

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Edwards Lifesciences LLC v. Cook Inc.</i> , 582 F.3d 1322 (Fed. Cir. 2009)	2
<i>Energizer Holdings, Inc. v. Int'l Trade Comm'n</i> , 435 F.3d 1366 (Fed. Cir. 2006)	9, 10
<i>Enzo Biochem Inc. v. Applera Corp.</i> , 780 F.3d 1149 (Fed. Cir. 2015)	16
<i>GPNE Corp. v. Apple Inc.</i> , 830 F.3d 1365 (Fed. Cir. 2016)	9, 14
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005)	3, 9, 14
<i>Sinorgchem Co., Shandong v. Int'l Trade Comm'n</i> , 511 F.3d 1132 (Fed. Cir. 2007)	2

Table of Defendants' Exhibits¹

Ex. No.	Exhibit / Publication Name
AA01	Excerpt from Prosecution History of U.S. Patent No. 7,446,338 – February 25, 2008 Amendment
AA02	Claim Construction Memorandum and Order, Solas OLED Ltd. v. Samsung Display Co. Ltd., et al., 2:19-cv-00152-JRG, Dkt. 99 (Apr. 17, 2020, E.D. Tex.)
AA03	Excerpts from Deposition of Richard A. Flasck, Solas OLED Ltd. v. Samsung Display Co. Ltd. et al., 2:19-cv-00152-JRG (Feb. 6, 2020, W.D. Tex.)
AA04	Solas's Proposed terms for Construction
AA05	Patent Owner's Preliminary Response, IPR2020-00320 (April 25, 2020, PTAB)
AA06	Solas Notice Of Agreement On Previously Disputed Claim Construction Terms, <i>Solas OLED Ltd. v. Samsung Display Co.</i> , 2:19-cv-00152-JRG, Dkt. 98 (E.D. Tex., April 15, 2020)
BB01	Prosecution History of European Patent Application No. 1,372,136
BB02	Prosecution History of U.S. Patent No. 7,499,042
BB03	Jiun-Haw Lee et al., Introduction to Flat Panel Displays 50-52 (John Wiley & Sons 2008)
BB04	Johnathan Halls, Short Course S-4: Fundamentals of OLEDs/PLEDs, S-4/101 (Society for Information Display, May 18, 2008)
DD01	Declaration of Richard A. Flasck in Support Of Solas's Responsive Claim Construction Brief, Solas OLED Ltd. v. LG, Ltd., et al, 6:19-cv-00236-ADA (Apr. 3, 2020, W.D. Tex.)
DD02	Solas's Reply Claim Construction Brief, Solas OLED Ltd. v. LG, Ltd., et al, 6:19-cv-00236-ADA (Apr. 24, 2020, W.D. Tex.)
DD03	Videoconference Deposition of Richard A. Flasck, Solas OLED Ltd. v. LG, Ltd., et al, 6:19-cv-00236-ADA, Dkt._82 (Apr. 14, 2020, W.D. Tex.)
DD04	Phillip A. Laplante, Comprehensive Dictionary of Electrical Engineering 213, 643 (Taylor & Francis Group, 2nd ed. 2005)
DD05	Stan Gibilisco, The Illustrated Dictionary of Electronics 179 (McGraw-Hill, 8th ed. 2001)
DD06	A Dictionary of Science 738-39 (Oxford University Press, 2006)
DD07	Steven M. Kaplan, Wiley Electrical and Electronics Engineering Dictionary 237 (John Wiley & Sons, Inc., 2004)
DD08	Collins Dictionary Electronics 139 (HarperCollins, 2007)
DD09	Erin McKean, The New Oxford American Dictionary 545 (Oxford University Press, 2nd ed. 2005)

¹ All exhibits were filed with Defendants' opening and responsive claim construction briefs. No additional exhibits are being filed with this reply brief.

Table Of Abbreviations For Citations To Parties' Briefs And Expert Declarations

Acronym	Document Description
Solas Open.	Solas's Opening Claim Construction Brief Filed as Dkt. 74 in the <i>Solas OLED Ltd. v. Google LLC</i> , Case No. 6:19-cv-00515-ADA ("Google Case")
Solas Resp.	Solas's Responsive Claim Construction Brief Filed as Dkt. 76 in the <i>Google Case</i>
Defs. Open.	Defendants' Opening Claim Construction Brief Filed as Dkt. 73 in the <i>Google Case</i>
Defs. Resp.	Defendants' Responsive Claim Construction Brief Filed as Dkt. 75 in the <i>Google Case</i>
Flasck Open. Decl.	Declaration of Mr. Richard Flasck Supporting Solas's Opening Brief Filed as Dkt. 74-2 in the <i>Google Case</i>
Flasck Resp. Decl.	Declaration of Mr. Richard Flasck Supporting Solas's Responsive Brief Filed as Dkt. 76-1 in the <i>Google Case</i>
Kanicki Open. Decl.	Declaration of Dr. Jerzy Kanicki Supporting Defendants' Opening Brief Filed as Dkt. 73-1 in the <i>Google Case</i>
Kanicki Resp. Decl.	Declaration of Dr. Jerzy Kanicki Supporting Defendants' Responsive Brief Filed as Dkt. 75-1 in the <i>Google Case</i>

I. U.S. Patent No. 7,446,338 (“338 Patent”)

A. “transistor array substrate” (claim 1)

Solas agreed to Defendants’ proposed construction in both the Eastern District of Texas and the PTAB, *see Ex. AA06; AA05 at 27–28*, and Solas’s statements to the PTAB constitute new intrinsic evidence supporting Defendants’ construction. Solas’s attempt to explain away its complete reversal is devoid of merit. Solas Resp. at 3. Solas now asserts that its statements to the PTAB were merely “pointing out the arguments that Samsung was presenting to the Board were inconsistent with the positions Samsung was taking in district court,” but that is plainly incorrect: Samsung Display took the same position in both the Eastern District and the PTAB. Indeed, pointing out a supposed “inconsisten[cy]” would not have required Solas to represent to the PTAB that it *agreed* to Defendants’ proposed construction, yet the fact is that Solas agreed to it and did so without qualification. Solas also has no explanation for how its representation to the Eastern District that it accepted Defendants’ proposed construction could be squared with its assertion that it was merely pointing out a purported “inconsisten[cy].” Simply put, if Solas had a substantive reason for disavowing the construction that it recognized to be appropriate just months ago, it would have offered one.

Defendants agree that the term “substrate” has a well-established meaning in the art, but Claim 1 does not recite a “substrate,” it recites a “transistor array substrate.” The difference is crucial, as the ’338 Patent discloses that a “substrate” is just one layer of the “transistor array substrate.” ’338 at 10:45–47 (“The layered structure from the insulating substrate 2 to the planarization film 33 is called a transistor array substrate 50.”). The claim specifies that the “transistor array substrate” also “comprises a plurality of transistors,” meaning that the “transistor array substrate” must contain transistors. Solas’s construction, which allows the transistors to be formed “upon” the transistor array substrate instead of within it, conflicts with the claim language.

Further, when a structure is formed *on* the transistor array substrate rather than within it, Claim 1 uses different language: *e.g.*, the “plurality of pixel electrodes” is arrayed “on the surface of the transistor array substrate.” And Solas’s proposed “clarification” of repeating the claim language “comprises a plurality of transistors” within the construction, Solas Resp. at 1–2, does not resolve the parties’ dispute, and results in a construction that is needlessly unclear.

The specification reinforces Defendants’ interpretation of the claim language and proposed construction. Solas cannot point to a single instance in which the “transistor array substrate” does not contain the array of transistors. Solas’s efforts to distinguish *Sinorgchem Co., Shandong v. Int'l Trade Comm'n*, 511 F.3d 1132 (Fed. Cir. 2007) also fail. Not only do Solas’s arguments about *Sinorgchem* fail to address the claim language here, *see* Solas Resp. at 2–3, they further disregard that the Federal Circuit in *Sinorgchem* found express definition and did not categorize use of the term “is” as “weaker evidence.” 511 F.3d at 1136. Solas’s attempt to distinguish *Edwards* is similarly unavailing. Solas Resp. at 3. The statement in *Edwards* was no more “categorical” than the statements of the ’338 Patent. *Id.* In fact, in *Edwards*, the Court explicitly found that “[c]ontrary to Edwards’s argument, the location within the specification in which the definition appears is irrelevant.” *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009) (finding that “the definition was not limited to the embodiment being discussed.”).

Finally, Solas constructs a strawman to argue that “[i]t is simply not true that one must be able to look at a single claim term such as ‘transistor array substrate’ in isolation and be able to find one and only one structure in an accused products that satisfies that claim term.” Solas Resp. at 2. This is not Defendants’ argument. Defendants showed Solas’s construction is fundamentally defective because it would provide no way to identify in a product what structures *are* a “transistor array substrate” and what structures are *not* part of the transistor array substrate. Solas fails to

address the fact that its construction would, if applied to the preferred embodiment of the '338 Patent, fail to include layers explicitly identified in the specification as part of the "transistor array substrate." *See* Defs. Open. at 5. Solas further fails to address, much less rebut, that its construction would leave indeterminate which layers would constitute a transistor array substrate.

B. "project from a surface of the transistor array substrate" (claim 1)

"The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc). Solas argues that "[n]othing in the claims refers to the interconnections serving as partition walls or preventing leakage." Solas Resp. at 4. But preventing leakage is a stated purpose of the invention, and Solas disregards that the language of the claim parallels the specification's description of the structure required to achieve that purpose. *See* '338 at 6:24-30, 6:38-42, 12:62-13:3. Solas's construction is inconsistent with this stated purpose. It is not surprising that Solas provides no support for its assertion that "[i]nterconnections that project from the local surface of the transistor array substrate can serve as partitions on that surface, even if there may be some other 'upper' surface elsewhere on the substrate," Solas's Resp. at 4, because there is no support for such an assertion in the '338 Patent.

II. U.S. Patent No. 7,499,042 ("042 Patent")

A. "selection period" (Claim 1)

Solas agrees with the key aspect of HP's construction: in each "selection period," a selection scan line must be *kept* active (or selected) during that entire period. Indeed, Solas rejects any suggestion that "the 'selection period' could encompass periods 'when a line or circuit is inactive and not selected.'" Solas Resp. at 14. Thus, the parties agree that the selection scan line *cannot* be inactive (or not selected) during any part of the "selection period."

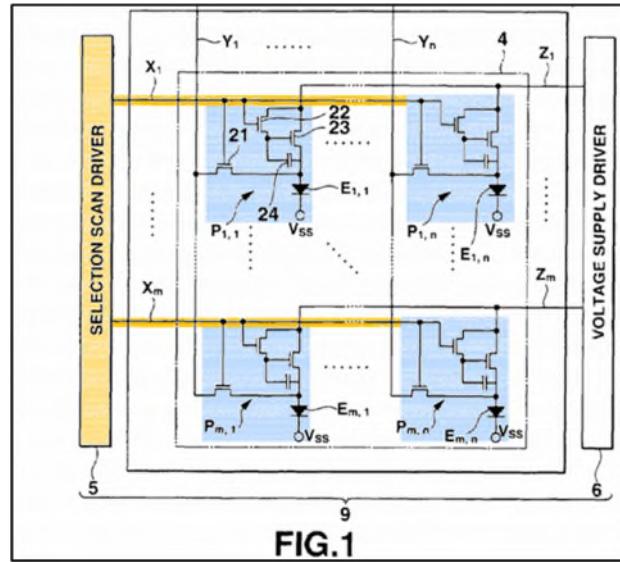
Solas's disagreement with HP's construction is based on trivial objections about word choice. Solas objects that the '042 Patent does not use the words "active" or "on" to describe the state of a "selection scan line," but instead uses the word "selected" or describes applying an "(ON-level) ON Voltage V_{ON} " to that line. *Id.* (citing '042 at 9:13-19). But there is no material difference between "active," "on," "selected," or applying an "ON Voltage V_{ON} " in the '042 Patent's context—these words all express the same concept. The specification, in fact, interchangeably refers to transistors being "ON" or "selected." *Compare* '042 at 9:5-12 ("selecting the first and second transistors"), *with* 10:23-27 ("transistor 23 is ON and the transistor 21 is OFF"). Solas itself acknowledges the equivalence of these words, given its objection to HP's construction as being redundant for using both "selected" and "active." Solas Open. at 18.²

What's more, Solas's objections regarding the proper usage of "selected" versus "active" are more applicable to its own proposal, which states "a plurality of pixel circuits is selected." But the specification never describes "pixel circuits" as being "selected." Instead, in the '042 Patent, each pixel circuit includes three transistors, and each transistor is *individually* selected or turned on. '042 at 9:5-12, 10:23-27. There is no notion of "select[ing]" a "pixel circuit(s)."

Solas also fails to justify its proposal of defining "selection period" with respect to "a plurality of pixel circuits," rather than with respect to a "selection scan line." Solas's briefs admit that the '042 Patent expressly defines a "selection period" with respect to a "selection scan line," stating: "a period in which the selection scan driver 5 . . . selects the *selection scan line* X_i in the i th row is called a *selection period*." *Id.* at 9:22–27; Solas Resp. at 15; Solas Open. at 17.

² To address Solas's semantic objections, HP is amenable to an alternative construction of "time duration in which a selection scan line is kept selected."

Solas nevertheless proposes deviating from this definition based on its assertion that a “selection scan line” comprises ‘a plurality of pixel circuits.’” Solas Resp. at 15. Solas’s assertion is plainly incorrect. As depicted in annotated Figure 1, each “selection scan line” (yellow) is a horizontal line that *connects* to a row of pixel circuits (blue). ’042 at 2:46-48 (“*a plurality of pixel circuits which are connected to the plurality of selection scan lines.*”). Thus, a



“selection scan line” is a separate structure from the “pixel circuits” to which the line connects. The “selection scan line” does not itself “comprise” any “pixel circuits.”

Further, by defining “selection period” to refer to when *any* “plurality of pixel circuits” are selected—not just “pixel circuits” connected to one “selection scan line”—Solas’s proposal places no limit at all on the duration of the “selection period.” *See* Defs. Resp. at 9. In fact, under Solas’s proposal the “selection period” refers to *any* time duration. This is because at any given time during the operation of an OLED display panel, the pixel circuits connected to one selection scan line are selected. Thus, a “plurality of pixel circuits is selected” at all times during operation. *Id.*

Solas also favors using “plurality of pixel circuits” over “selection scan line” in the construction because the latter phrase is used elsewhere in Claim 1 and therefore allegedly redundant. Solas Resp. at 15. But Solas’s concern over redundancy applies equally to its own proposal—the phrase “plurality of pixel circuits” appears three times in Claim 1. Thus, following the specification, “selection period” should be defined with respect to a “selection scan line.”

B. “sequentially selects said plurality of selection scan lines in each selection period” (Claim 1)

Solas’s briefs argue that (1) no construction is required for this disputed 12-word term because it “includes only words and phrases that have a plain and ordinary meaning” and (2) HP’s construction limits the claim to an “exemplary embodiment” based on a “singular statement in the specification.” Solas Open. at 19; Solas Resp. at 17. Solas is wrong on both counts.

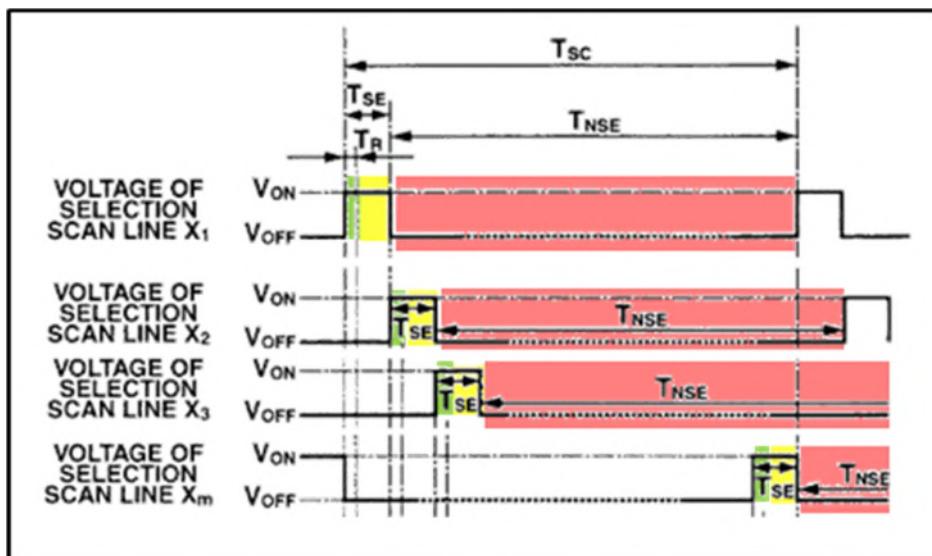
First, the disputed term lacks any ordinary meaning outside the context of the ’042 Patent. Not only does the term include technical phrases coined by the ’042 Patent (*e.g.*, “selection period”), but its meaning is unclear on its face without context. In particular, it is ambiguous whether one or a plurality of “selection scan lines” is selected in each “selection period.”

Second, the claim’s ambiguity is resolved by context from the specification, which makes clear that (a) each “selection scan line” is active during its own “selection period,” and (b) only one “selection scan line” can be active at a time—as a result, the “selection periods” of multiple selection scan lines must be *non-overlapping* in time. *See* Defs. Open. at 11-12. The specification’s context goes well beyond the “singular” and unequivocal statement that Solas identifies: “the *selection periods* T_{SE} of the selection scan lines X_1 to X_m do not overlap each other.” ’042 at 9:29-31. The specification’s context further includes *every* embodiment. Indeed, the specification explains that “selection scan lines” are “individually” selected so that “while applying the ON voltage V_{ON} to the selection scan line X_i , the selection scan driver 5 applies the OFF voltage V_{OFF} to the other selection scan lines X_1 to X_m (except for the selection scan line X_i).” *Id.* at 9:13-19, 9:26-29, Fig. 4. Thus, at any given time, only one “selection scan line” can be selected or “ON” while all other lines are de-selected or “OFF.” There is no contrary suggestion in the ’042 Patent that two or more “selection scan lines” could be on at the same time and have overlapping “selection periods,” and Solas identifies none.

C. “designating current” (Claim 1)

Solas’s arguments opposing construing “designating current” to require a “constant” current value demonstrate a fundamental misunderstanding of the ’042 Patent. As shown in annotated Figure 4 below, the ’042 Patent programs and displays a unique brightness level to each pixel through a cyclical, three-step process. First, in a period known as the “reset period T_R ” or the “first part of the selection period” (green), a “reset voltage” is applied, clearing the brightness level stored on the pixel from the prior cycle.

’042 at 11:50-12:15, Claim 1 (“appl[ying] a reset voltage . . . in a first part of the selection period”). Next, in the “second part of the



selection period” (yellow), a “designating current” I_{DATA} is applied, which programs the brightness level of the pixel. *Id.* at 11:41-57, Claim 1 (“suppl[ying] a designating current . . . in a second part of the selection period”). Finally, in the “non-selection period” T_{NSE} (red), the programmed brightness level is displayed. *See id.* at 10:44-47. Each of these three steps occur in one cycle called a “frame period T_{SC} ,” where one brightness level is programmed and displayed. *See id.* at 9:53-57. Over many cycles or frame periods, a pixel can be programmed to display many different brightness levels, with one level programmed and displayed in each cycle. *See id.*

The critical point is that across the time periods shown in Figure 4, the “designating current” I_{DATA} *only exists in the second part* of the “selection period” T_{SE} . During this time “the current value of the tone designating current I_{DATA} [is held] constant” “in accordance with the

image signal for each selection period T_{SE} of each row.” *Id.* at 11:41-57. The “designating current” does not exist—and therefore does not have any value (constant or otherwise)—during the first “reset” subperiod or in the later “non-selection period.” *Id.* at 12:16-21; *see* Defs. Resp. at 13-14.

With the foregoing context in mind, Solas’s arguments are irrelevant misdirection. First, while Solas acknowledges that the “designating current I_{DATA} [is] *constant* in a period from the end of each reset period T_R to the end of the corresponding selection period T_{SE} ,” it argues that the “specification never describes the designating current as being held constant during the first reset portion of the selection period.” Solas Resp. at 19 (citing ’042 at 11:47-59). As explained above, however, the “designating current” *does not even exist* in the “first reset portion of the selection period.” Instead, as the specification states, the “designating current” *only exists* in the selection period’s second portion, which starts from the “*end* of each reset period T_R ” and continues to “the end of the corresponding selection period T_{SE} .” ’042 at 11:50-57.

Second, Solas states that the “designating current” has a value “corresponding to an image signal.” Solas Resp. at 19-20. This is true, but it has no relevance to whether the “designating current” is held constant. To the extent Solas is implying that an “image signal” has a brightness level that varies over time, any such variations occur between *multiple* cycles, not within one cycle. But Claim 1 and HP’s construction concern what happens in *one* cycle. And in each cycle, a new “designating current” with constant value is generated to represent the image signal.

Third, Solas completely misreads its other cited evidence, column 16:31-32 and Figure 9, for reasons already explained in detail in Defendants’ response brief. Defs. Resp. at 14-15.

D. “current lines” (Claim 1)

Solas’s proposal and arguments for “current lines” present an example of its flawed understanding of plain and ordinary meaning. Plain meaning is not the meaning based on an

attorney’s say-so or a lay juror’s understanding. Rather, it is the meaning to a person of ordinary skill after considering the “context of the written description.” *Phillips*, 415 F.3d at 1313, 1321.

In the context of the ’042 Patent and all its embodiments, as detailed in Defendants’ briefs, the “current lines” are conductive lines, where each individual “current line” connects to a line of pixel circuits. Defs. Resp. at 15-16. Indeed, the specification consistently refers to the “current lines” as “current lines Y_1 to Y_n ” or “current line Y_j ” over 100 times across embodiments, where “ Y ” denotes the vertical lines in the patent’s figures, each connecting to a column of pixel circuits. *E.g.*, ’042 at 5:12-20, Figs. 1, 3, 10-12. In *GPNE Corp. v. Apple Inc.*, the Federal Circuit construed “node” as “pager” because the specification “repeatedly and exclusively” used “pager” “over 200 times . . . to refer to the devices in the patented system.” 830 F.3d 1365, 1370-71 (Fed. Cir. 2016) . Similarly, “current lines” should be construed consistently with the specification’s repeated use of that term to refer to the specific “current lines Y ,” each of which connects to a column of pixels.

Construing “current lines” to refer to any “conductive lines for carrying current,” as Solas proposes, places no bounds on the term because every “conductive line” is “for carrying current.” As a result, Solas’s proposal for “current lines” encompasses other types of lines that the specification never calls “current lines,” including lines internal to only a single pixel circuit.

III. U.S. Patent No. 7,663,615 (“615 Patent”)

A. “the operation” (Claim 11)

In both of its briefs, Solas admits that “*the operation*” lacks antecedent basis. Solas Resp. at 22; Solas Open. at 24. Solas, however, insists that “lack of antecedent basis does not render a claim indefinite so long as here the term has a ‘reasonably ascertainable meaning,’ which ‘must be decided in context,’” citing *Energizer Holdings, Inc. v. Int’l Trade Comm’n*, 435 F.3d 1366, 1370 (Fed. Cir. 2006). Solas Resp. at 22. But in *Energizer*, the term lacking express antecedent

basis, “said zinc anode,” closely resembled another limitation in the claim, “*anode* gel comprised of *zinc*,” which provided implicit antecedent basis. 435 F.3d at 1369-71.

By contrast, “the operation” bears no resemblance to the 36-word phrase that Solas identifies. Solas argues that “the operation” and the 36-word phrase are interchangeable, though, because “the operation” is performed by the “light emission control section,” and “the operation” must “refer to the earlier—and *only*—recitation of what the light emission control section does,” which is the 36-word phrase in Solas’s proposal. Solas Resp. at 22-23 (emphasis original). As discussed in Defendants’ response brief, Solas’s argument hinges on an incorrect premise: that there is only one, definitive “operation” that the “light emission control section” performs and that “operation” is captured by Solas’s 36-word proposal. Defs. Resp. at 19-20.

The specification refutes Solas’s premise, showing instead that the “light emission control section” performs many different “operations.” As detailed in Defendants’ briefs and its expert Dr. Kanicki’s declarations, the specification describes at least seven different “operations,” including: “precharge operation,” “threshold correction operation,” “writing operation,” “light emission operation,” “drive control operation,” “display operation,” and “gradation sequence display operation.” *E.g.*, Defs. Resp. at 17-20; Kanicki Resp. Decl. at ¶¶9-16. Critically, the “light emission control section”³ performs *every* one of the many different “operations.” *Id.* Thus, no one “operation” can be characterized as “*the* operation” of the “light emission control section.”

Further, the many functions that the light emission control section performs across its many “operations” in the specification far exceed the two operations described in Solas’s 36-word

³ The parties agreed to construe “light emission control section” as “drive transistor.” Solas Op., Ex. 7 (joint chart). In the specification, the “drive transistor” (element Tr13) actively performs many different “operations.” *E.g.*, ’615 at 20:12-30 (Tr13 performing “precharge operation”), 21:35-52 (Tr13 performing “threshold correction operation”), 24:5-28 (Tr13 performing “writing operation”), 25:41-53 (Tr13 performing “light emission operation.”).

proposal. *Id.* Solas is therefore incorrect in suggesting that a “POSITA would clearly understand ‘the operation’” to refer to the 36-word phrase. Solas Resp. at 22. In truth, a POSITA would find Solas’s choice of the 36-word phrase as “the operation” arbitrary given the many other “operations” that the “light emission control section” performs.

Solas distinguishes the cases cited in HP’s brief by claiming that unlike the plaintiffs in those cases, Solas is not trying to correct the claims to fix an antecedent basis issue, but it is instead proposing “plain and ordinary meaning” and asking the Court for “clarification in its ruling or a footnote” about what “the operation” means. Solas Resp. at 23-24. But Solas’s request for “clarification” is simply a backdoor way of correcting Claim 11’s indefiniteness problem by construing “the operation” as 36 different words. If the meaning of “the operation” were so clear, no clarification would be necessary. Further, Solas’s supposed “plain and ordinary meaning” proposal is anything but. The plain meaning of “the operation” is not Solas’s 36-word proposal.

B. “precharge voltage” (Claim 11)

Solas concedes that while Claim 11 recites only one “precharge voltage,” the specification discloses two different types of “precharge voltages”: (1) “V_{pre}” and (2) “V_{pre13}.¹³” Solas Resp. at 25. Solas nonetheless contends that there is no ambiguity over what “precharge voltage” means because it “corresponds to the ‘precharge voltage V_{pre},’ and not V_{pre13}.¹⁴” *Id.* at 25-26.

Solas’s choice of V_{pre}—rather than V_{pre13}—as the claimed “precharge voltage,” however, is arbitrary and premised on two flawed arguments. First, Solas argues that V_{pre13} is not a “precharge voltage” because “V_{pre13} is consistently referred to as the ‘**drive transistor precharge voltage V_{pre13}**’ . . . V_{pre13} is never referred to as the ‘precharge voltage.’” Solas Resp. at 25 (emphasis original). Solas’s own quote defeats its assertion: “V_{pre13}” is preceded by the label “precharge voltage.” The additional prefix of “drive transistor” does not somehow remove or alter the “precharge voltage” label. Thus, V_{pre13} is referred to as “precharge voltage.”

Second, according to Claim 11, the “precharge voltage” must have *two* characteristics: (1) it is applied by the “data driver” to the “data line” and (2) it has a value that “exceed[s] a threshold value of the drive transistor.” *See* ’615 at Claim 11 (“the data driver applies a *precharge voltage exceeding a threshold value of the drive transistor* to the data line”); Defs. Open. at 19-21; Defs. Resp. at 20-22. But Solas and its expert Mr. Flasck only describe how V_{pre} satisfies the first characteristic: that it is applied to the data line. Solas Resp. at 26; Flasck Resp. Decl. ¶¶22–24. They make no attempt to show that V_{pre} satisfies the second characteristic “exceeding a threshold value of the drive transistor.”

Solas’s and Mr. Flasck’s omission is not surprising: the specification provides no suggestion that V_{pre} exceeds the threshold value of the drive transistor. By contrast, the specification repeatedly explains that the other precharge voltage—V_{pre13}—exceeds the threshold value, also called “V_{th13}.” For example, the specification states a “*V_{pre13} that is larger than the threshold V_{th13}* of the drive transistor Tr 13 is applied” and “the voltage V_{pre13} is higher than the threshold voltage V_{th13}.” ’615 at 20:63-67, 19:7-9, Fig. 3A (showing “V_{pre13} > V_{th13}”).

But while V_{pre13} exceeds V_{th13}, it does not satisfy the first characteristic of being applied to the data line. Thus, Claim 11’s “precharge voltage” does not correspond to V_{pre}, V_{pre13}, or anything else in the specification. As a result, a person of ordinary skill could not determine with reasonable certainty the scope of the “precharge voltage,” rendering Claim 11 indefinite.

C. “writing control section” (Claim 11)

As with other terms, Solas not only refuses to meaningfully engage with the intrinsic record; it dismisses HP’s discussion of the intrinsic record as “import[ing] limitations from embodiments.” Solas Resp. at 28-29. But for “writing control section,” the two aspects of HP’s construction that Solas opposes—(1) controlling writing of a “precharge voltage” and (2) specifying that the structure of the section is a “transistor”—do not come from embodiments. The

first aspect comes from Claim 11’s language, which recites “the light emission drive circuit *applies the precharge voltage . . . via the writing control section.*” This limitation means that the “write control section” is the structure through which the “precharge voltage” is applied and written, consistent with HP’s construction. The second aspect, that the structure of this section is a “transistor,”⁴ comes from the specification’s express definition. The specification uses an equivalent term “writing control means” to refer to a “selection transistor”: “a light emission drive circuit DC according to the invention is configured so as to have: a *selection transistor (writing control means)* Tr 12.” ’615 at 17:7-9.

Solas also fails to rebut that its proposal, “circuit section that controls writing,” erases any distinction between the “writing control section” and the other “sections” in Claim 11 that also “control writing.” Solas only contends that other, *surrounding claim language* sufficiently differentiates “writing control section” from the other “sections.” Solas Resp. at 27-28. But Solas’s contention merely proves HP’s point. To be consistent with the surrounding language, “writing control section” should be construed to differentiate it from the other “sections.” Solas’s proposal, however, has the opposite effect and therefore contravenes the surrounding claim language. Indeed, under Solas’s proposal, the same structure could be read on both the “writing control section,” and either one of the “light emission control section” or “voltage control section,” given that each of the latter two “sections” also “controls writing.”

D. “data lines” (Claim 11)

Solas’s proposal and arguments for “data lines” present another example of its flawed understanding of ordinary meaning. A term’s ordinary meaning is not its meaning in dictionaries,

⁴ Solas’s argument that it is improper to limit a “section” to a “transistor” is belied by its agreement to construe “light emission control section” as “drive transistor.” Solas Op., Ex. 7 (joint chart).

which Solas cites as its main support for its proposal. Rather, it is the meaning to a person of ordinary skill after considering the “context of the written description.” *Phillips*, 415 F.3d at 1321.

In the context of the ’615 Patent and all its embodiments, the “data lines” are conductive lines, where each individual “data line” connects to a column of pixel circuits, as detailed in Defendants’ briefs. Defs. Resp. at 24-25. Indeed, the specification consistently refers to the “data lines” as “data line[s] DL” over 50 times, where “DL” denotes the vertical lines, each connecting to a column of pixel circuits, in the patent’s figures. *E.g.*, ’615 at Figs. 1, 16. In *GPNE*, the Federal Circuit construed “node” as “pager” because the specification “repeatedly and exclusively” used “pager” “over 200 times . . . to refer to the devices in the patented system.” 830 F.3d at 1370-71. Similarly, “data lines” should be construed consistently with the specification’s repeated use of that term to refer to the specific “data line[s] DL,” each of which connects to a column of pixels.

“Data lines” should not, on the other hand, be construed based on Solas’s single dictionary definition of an unrelated term, “data *transmission* line,” as “[a] system of electrical conductors, such as a coaxial cable or pair of wires, used to send information.” Solas Open. at 27; *id.* at Ex. 10 at 490 (underlining added). Indeed, the underlined portion, which Solas omits from its briefs, reveals that the definition has no applicability to the ’615 Patent and OLED circuits because “data lines” in such circuits are not coaxial cables or wire pairs.

Finally, Solas’s proposal to replace “data” in the term with “information” derives from its inapplicable dictionary definition and should be rejected on that basis alone. Moreover, “information” and “data” are not the same. “Data” in the context of OLEDs and the ’615 Patent refers specifically to “*display data*” (or “gradation sequence current I_{DATA} ”) that affects the luminance or brightness displayed by a pixel. *E.g.*, ’615 at 25:67-26:2. By contrast, “information” encompasses control signals sent on other types of conductive lines that Claim 11 recites separately

using different names. Claim 11 recites sending “voltage *control* signals” on “*hold* lines” and “writing *control* signals” on “*selection* lines.” Solas’s use of “information” would erase any distinction between “data lines” and those distinct other types of lines in Claim 11.

IV. U.S. Patent No. 7,573,068 (“’068 Patent”)

- A. “formed on said plurality of supply lines along said plurality of supply lines” (Claim 1) / “connected to said plurality of supply lines along said plurality of supply lines” (Claim 13)**

After two rounds of briefing, Solas has not disputed that the ’068 Patent discloses and enables *only* two methods by which feed interconnections are “formed on” or “connected to” supply lines: (1) stacking the feed interconnection on top of the supply line over its length (Figures 1, 2, and 8), or (2) a grid formation in which the feed interconnections make multiple contacts with the plurality of supply lines over the length of each line (Figures 20 and 21). Defs. Open. at 24-28; Solas Resp. at 6-10. Indeed, Solas’s expert Mr. Flasck agrees that there are “two relevant embodiments,” and he describes both in the same manner as Defendants: (1) a “first embodiment (Figs. 1 and 2),” where “each feed interconnection[] 90 runs parallel to and is connected to one of the supply lines” and (2) a “second embodiment (Figs. 20 and 21),” where “each feed interconnection 90 crosses and connects to each supply line.” Flasck Open. Decl. at ¶¶88-90. Solas also agrees that in light of the two embodiments, the disputed terms do not permit a feed interconnection and a supply line to connect at just “a single arbitrary point.” Solas Resp. at 8.

Despite its agreement, Solas’s constructions use a phrase, “length or direction,” that is ambiguous and incorrect to the extent that it encompasses the possibility of a supply line connecting to a feed interconnection at only a single point. Solas argues that its construction does not encompass this single contact arrangement (which it tacitly admits is not disclosed or enabled), but the plain language of Solas’s constructions are not limited as Solas claims—it potentially opens the door to Solas later arguing that a single contact arrangement is within the scope of the claims.

Solas attacks Defendants' construction by accusing it of improperly importing limitations from the patent's two embodiments. But Solas's attack is curious given that its own expert freely admits that these are the "two relevant embodiments" as to how feed interconnections are "formed on" or "connected to" supply lines in the '068 Patent. The only construction that accurately captures those two embodiments is that which Defendants have proposed.

Solas's remaining attacks against Defendants' construction are superficial. For instance, Solas argues that Defendants' construction is "suspect because it assigns the *identical construction* to both [formed on and connected to] terms." Solas Resp. at 7-8. Solas has not, however, identified any instance where the '068 Patent ascribes different meanings to "formed on" and "connected to," and its expert confirms that the terms have no material difference. Flask Open. Decl. ¶91.

Solas also critiques Defendants' construction by noting that the plain English meanings of "formed on" or "connected to" are readily understood. Solas Resp. at 7. Even if true, for purposes of claim construction, those words must be considered in the context of the '068 Patent. The phrases alone do not identify to a person of skill in the art *how* specifically the feed interconnections must be "formed on" or "connected to" supply lines in the claims. The parties agree that not every possible formation or connection of feed interconnections and supply lines are claimed in the '068 Patent. Defs. Open. at 28; Solas Resp. at 8. Thus, the purported plain English meanings of "formed on" or "connected to" are not sufficient.

Finally, Solas downplays the '068 Patent's objectives—*i.e.*, improving the conductivity of the supply lines, and avoiding voltage drops and signal delays—as simply "benefits." Solas Resp. at 9. These are not simply "benefits," however; they are the purpose of the alleged invention and affect the scope of the claims. *See, e.g., Enzo Biochem Inc. v. Applera Corp.*, 780 F.3d 1149, 1156 (Fed. Cir. 2015) (adopting a narrower claim construction because the specification "clearly

indicate[d] that the purpose of the invention was directed” to a narrower invention). The reason for that is because improving the conductivity of the supply lines (and avoiding related problems of voltage drops and signal delays) requires having sufficient contacts between those lines and feed interconnections. Defs. Open. at 28; Defs. Resp. at 27-28. Having just a single point of contact between a supply line and a feed interconnection would not achieve the patent’s objectives, as Solas’s expert Mr. Flasck conceded. Defs. Open. at 28, Ex. DD03 at 213:19-215:10; Solas Resp. at 9. Because only Defendants’ construction reflects this objective, it should be adopted.

B. “signal lines” / “supply lines” (Claims 1, 13)

Solas falsely claims that Defendants have argued that Solas’s constructions of “signal lines” and “supply lines” are “inconsisten[t]” or in “tension” with each other. Solas Resp. at 4-5. Defendants, however, have argued the exact opposite—instead of being inconsistent, Solas’s two constructions of the two distinct terms are substantively the same, and thus fail to differentiate “signal lines” from “supply lines.” In fact, Solas’s constructions would allow it to argue that any electrical line supplying a current or voltage is a “signal line” *or* a “supply line,” as it sees fit. Although Solas maintains that its constructions for “signal lines” and “supply lines” are not interchangeable, it has not been able to articulate any cogent difference between them.

Indeed, Solas’s attempts to identify differences between its two constructions has the opposite effect. Solas proposes a circular definition for “signal lines” (“conductive lines supplying signals”) and defines “supply lines” as “conductive lines supplying current or voltage.” Solas Resp. at 5. Solas insists that the two proposals are different because a “signal” “is not identical to ‘current or voltage.’” *Id.* But the lone support that Solas cites is a dictionary definition that directly contradicts its position: “**signal** n. 1. Any electrical quantity, such as **voltage**, **current**, or frequency, that can be used to transmit information.” *Id.* (emphasis added). Thus, a “signal” is defined as a “voltage” or “current,” confirming their equivalence. And because a “voltage [or]

“current” can be a “signal,” Solas’s two constructions using these phrases are interchangeable—any voltage or current supplied on an electrical line satisfies both constructions.

After failing to defend its two constructions as different, Solas later backtracks and claims that “different terms can have similar or synonymous meanings.” Solas Resp. at 5. Even ignoring that Solas cites no legal authority for this contention, Solas does not provide any explanation for why the two terms at issue here—“signal lines” and “supply lines”—should have similar or synonymous meanings in the context of the ’068 Patent. Solas does not dispute that the two lines perform different functions in the ’068 Patent. And Solas acknowledges that the two lines have different structures, stating that: “claim 1 requires the signal lines to be patterned together with the gates of driving transistors, whereas the supply lines are patterned together with the sources and drains.” *Id.* “Signal lines” and “supply lines” cannot have the same meaning.

Finally, Solas’s response brief repeats the same flawed attacks from its opening brief regarding Defendants’ construction of “supply lines.” Solas argues that Defendants’ construction of “supplying a driving current or voltage” is wrong because the ’068 Patent describes supplying other types of signals, like a “clock signal,” on the supply lines. Solas Resp. at 6. But as Defendants have explained, Solas is mischaracterizing Defendants’ construction as being limited to *only* supplying a driving current or voltage. Defs. Resp. at 30-31. In truth, nothing in Defendants’ construction prevents supply lines from supplying a “clock signal,” so long as that line is *also* capable of supplying a driving current or voltage. *Id.* Solas also repeats its contention that Defendants’ construction is based on “optional embodiments” where a supply line connects to a “plurality of pixel circuits.” Solas Resp. at 6. In fact, every embodiment discloses each supply line connected to multiple pixel circuits. There is no contrary embodiment or disclosure of a supply line connected to only a single pixel circuit, and Solas has identified none.

C. “source” / “drain” (Claims 1, 13)

Solas’s response brief confirms that plain and ordinary meaning is inadequate here. In fact, Solas’s criticism of various dictionary definitions of “source” and “drain” as inconsistent (*see* Solas Resp. at 11) only confirms that plain and ordinary meaning is inappropriate because there are no consistent, well-understood definitions of those terms in the art. Thus, leaving those terms unconstrued would leave unsettled which structures within a thin film transistor (TFT) are encompassed by the ordinary meaning of “source” and “drain.”

Rather than address this deficiency with ordinary meaning, Solas spends most of its briefs criticizing Defendants’ constructions for using the word “electrode.” Solas Resp. at 10-11. But as Defendants’ response brief detailed, Solas and Defendants, in fact, agree that “source” and “drain” refer to conductive film structures labeled 23s and 23d in Figure 5 of the ’068 Patent. Defs. Resp. at 33-34. While Defendants prefer to call these structures “source electrode” and “drain electrode” for short, Solas and its expert Mr. Flasck have simply defined those same structures with a longer phrase: “the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region.” Flasck Open. Decl. at ¶101; Solas Resp. at 11. Although Defendants maintain that the term “electrode” is correct and sufficient as shorthand for Solas’s definition (*see* Defs. Open. at 31; Defs. Resp. at 32-34), in an effort to eliminate any dispute, Defendants reiterate that an appropriate alternative construction of “source” and “drain” is one that follows Solas’s definition: “the patterned conductive film that is connected to one end of the TFT channel region through a doped semiconductor region.”⁵

⁵ To resolve the parties’ disputes regarding “source” and “drain,” Defendants has asked Solas to agree to Solas’s expert Mr. Flasck’s definition of those terms as the construction. To date, Solas has not responded to Defendants’ repeated requests.

DATED: July 30, 2020

By: /s/ Michael D. Jay
JOHN M. GUARAGNA
Texas Bar No. 199277
john.guaragna@dlapiper.com
DLA PIPER LLP (US)
401 Congress Avenue, Suite 2500
Austin, TX 78701-3799
Tel: 512.457.7000
Fax: 512.457.7001

MICHAEL D. JAY (*pro hac vice*)
Bar No. 223827
michael.jay@dlapiper.com
NANDAN R. PADMANABHAN (*pro hac vice*)
Bar No. 280309
nandan.padmanabhan@dlapiper.com
DLA PIPER LLP (US)
2000 Avenue of the Stars
Suite 400 North Tower
Los Angeles, California 90067-4704
Tel: 310.595.3000
Fax: 310.595.3300

MARK FOWLER (*pro hac vice*)
Bar No. 124235
mark.fowler@dlapiper.com
DLA PIPER LLP (US)
2000 University Avenue
East Palo Alto, CA 94303-2214
Tel: 650.833.2000
Fax: 650.833.2001

Attorneys for DEFENDANT APPLE INC.

By /s/ Mark Liang
Melissa R. Smith
Texas Bar No. 24001351
GILLAM & SMITH, LLP
303 South Washington Avenue
Marshall, Texas 75670
Tel: (903) 934-8450
Email: melissa@gillamsmithlaw.com

Ryan K. Yagura
Texas Bar No. 24075933
Nicholas J. Whilt
Brian M. Cook
Boris Mindzak
O'MELVENY & MYERS LLP
400 South Hope Street, 18th Floor
Los Angeles, CA 90071
Telephone: 213-430-6000
Email: ryagura@omm.com
Email: nwhilt@omm.com
Email: bcook@omm.com
Email: bmindzak@omm.com

Darin W. Snyder
David S. Almeling
Mark Liang
O'MELVENY & MYERS LLP
Two Embarcadero Center, 28th Floor
San Francisco, CA 94111
Telephone: 415-984-8846
Email: dsnyder@omm.com
Email: dalmeling@omm.com
Email: mliang@omm.com

ATTORNEYS FOR DEFENDANT HP INC.

By /s/ Mark Liang
Michael E. Jones
SBN: 10929400
POTTER MINTON, PC
110 North College, Suite 500
Tyler, TX 75702
Tel: 903-597-8311
Fax: 903-593-0846
mikejones@potterminton.com

Ryan K. Yagura
Texas Bar No. 24075933
Nicholas J. Whilt
Brian M. Cook
Boris Mindzak
O'MELVENY & MYERS LLP
400 South Hope Street, 18th Floor

Los Angeles, CA 90071
Telephone: 213-430-6000
Email: ryagura@omm.com
Email: nwhilt@omm.com
Email: bcook@omm.com
Email: bmindzak@omm.com

Darin W. Snyder
David S. Almeling
Mark Liang
O'MELVENY & MYERS LLP
Two Embarcadero Center, 28th Floor
San Francisco, CA 94111
Telephone: 415-984-8846
Email: dsnyder@omm.com
Email: dalmeling@omm.com
Email: mliang@omm.com

**ATTORNEYS FOR DEFENDANT
GOOGLE LLC**

By s/ Melissa R. Smith _____

Melissa R. Smith
Texas Bar No. 24001351
GILLAM & SMITH, LLP
303 South Washington Avenue
Marshall, Texas 75670
Tel: (903) 934-8450
Email: melissa@gillamsmithlaw.com
Fax: (903) 934-9257

Jeffrey H. Lerner
jlerner@cov.com
David A. Garr
dgarr@cov.com
Jared R. Frisch
jfrisch@cov.com
Grant D. Johnson
gjohnson@cov.com
Daniel W. Cho
dwcho@cov.com
COVINGTON & BURLING LLP
One CityCenter

850 Tenth Street, NW
Washington, DC 20001-4956
Phone: (202) 662-6000
Fax: (202) 662-6291

Robert T. Haslam
rhaslam@cov.com
COVINGTON & BURLING LLP
3000 El Camino Real
5 Palo Alto Square, 10th Floor
Palo Alto, CA 94306-2112
Phone: (650) 632-4700
Fax: (650) 632-4800

**COUNSEL FOR DEFENDANT DELL
INC.
AND INTERVENOR SAMSUNG
DISPLAY CO., LTD.**

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document on July 30, 2020.

/s/ Michael D. Jay
Michael D. Jay